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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/707,060	11/06/2000	Branko Kovacevic	ATI000069	5798

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EXAMINER	
ONUAKU, CHRISTOPHER O	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/707,060	KOVACEVIC, BRANKO	
	Examiner	Art Unit	
	Christopher Onuaku	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-20* is/are allowed.

6)☒ Claim(s) *1-17 and 21-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-17&21-27 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 21-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki (US 6,148,135).

Regarding claim 21, Suzuki discloses a video and audio synchronization controller for decoding coded video and audio data and for synchronizing video data with audio data and a video decoding device in the video and audio reproducing device for preventing the video buffer memory from becoming empty (underflow) or full (overflow), comprising:

a) a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs (see Fig.4, video and audio separator 2 which receives coded video and audio data 1; col.8, lines 35-60);

b) a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data (see Fig.4, video and audio separator 2 which receives coded video and audio data 1; col.8, lines 35-60; and col.9, lines 20-32), here video and audio packets are disclosed and each packet has a frame header, and each video and audio packet header includes vide presentation time stamp

c) a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets (see Fig.4; video buffer memory 45 and audio buffer memory 25; col.8, line 61 to col.9, line 14);

d) a first clock recovery module having an input coupled to the first input node, and an output, wherein the clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before it is stored in the storage device (see Fig.1; system counter 101; system clock reference 3 and system tine clock 102; col.10, lines 6-55); and

e) a decoder having a first input coupled to the output of the first clock recovery system to receive the clock, a second input coupled to the data port of the storage

device to receive the select packets, and an output to provide decoded real-time data (see Fig.4; video decoder 50 and audio decoder 30; col.8, line 61 to col.9, line 14).

Regarding claim 22, Suzuki discloses wherein the first clock recovery module further generates the clock based upon data transmitted in packets of a currently received multiplexed packetized data stream (see Fig.1; system time counter 101 and system clock reference 3; col.10, lines 6-55).

Regarding claim 23, Suzuki discloses wherein the first clock recovery module further generates the clock based upon multiplexed packetized data stream data stored in the storage device (see Fig.1; system time counter 101 and system clock reference 3; col.10, lines 6-55), here the SCR 3, the video time stamp and the video data packet are received by the video and audio separator 2 and stored in the video buffer memory, for example.

Regarding claims 24&25, Suzuki discloses wherein the decoder includes a video decoder and wherein the decoder includes an audio decoder (see Fig.; video decoder 50 and audio decoder 30; col.8, line 61 to col.9, line 14).

Regarding claim 26, Suzuki discloses a second transport stream demultiplexer having an input coupled to the data port of the storage device (see Fig.14; and audio and video separator 2; video buffer memory 45 and audio buffer memory 25; col.8, line

36 to col.9, line 14) here Suzuki discloses that the receiver of Fig.4 can be used to receive video and audio from satellite or cable communication lines, and in any of the cases the audio and video separator 2 serves as a 'second' demultiplexer.

Regarding claim 27, Suzuki discloses a second clock recovery module having an input coupled to the data port of the storage device to allow STC setting based on the stored system time (see Fig.1, system time clock counter 101 and STC 102, wherein the system time clock counter counts up the the updated system time clock (STC) 102 by setting to the count of the system clock reference 3 which is inckuded in the header of the video frame; col.10, lines 32-55).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (US 6,148,135).

Regarding claim 1, Suzuki discloses a video and audio synchronization controller for decoding coded video and audio data and for synchronizing video data with audio data and a video decoding device in the video and audio reproducing device for

preventing the video buffer memory from becoming empty (underflow) or full (overflow), comprising the method of:

a) receiving a mnultiplexed packetized data stream that carries real-time multimedia programs (see Fig.4 which is used as a receiver that receives video and audio data pasckets; col.8, lines 49-60);

b) storing a first portion of the packetized data stream representing video data and timing of a program (see Fig.4, video buffer memory 45; col.8, lines 61-67), here video buffer memory stores the received video data;

c) setting a system time indicator (clock) to a stored system time value, wherein the stored system time value is based on a portion of the timing data of the first portion of the packetized data stream (see Fig.1, selector 110, system time counter 101, video synchronization comparator 109 and audio synchronization comparator 103; col.10, lines 6-23), here the selector 110 selects either the system clock reference (SCR) 3 or the delayed video time stamp (V-TS) 49. The system time counter sets the timing according to the output from the selector 110, counts the clocks, and generates and outputs the system time clock (STC) 102;

d) incrementing the system time indicator (see col.10, lines 33-55), here selector 110, selects SCR 3 and updates system time counter 101 by the count of the system clock reference 3. The system clock reference 3 is contained in the headers of the respective frames in the coded video and audio data, and is a reference clock transmitted from the transmitting terminal to provide the system with the absolute time periodically;

d) retrieving the video data of the first portion of the packetized data stream for video decoding (see Fig.4, col.8, line 61 to col.9, line 3), here the coded video data 41 and video time stamp 42, stored in the video buffer memory 45, are output from the video buffer memory 45 to the video decoder 50, and in col.11, lines 10-48, the decoding process is detailed.

Suzuki fails to explicitly disclose storing a second portion of the packetized data stream representing video data and timing data of the program, which examiner reads as the output of the video decoder 50 of Fig.4. Official Notice is taken that it would have been obvious to modify Suzuki by adding a storage means to Suzuki in order to store the decoded video and timing data output of the video decoder 50

Regarding claim 2, Suzuki discloses the method wherein:

a) storing the first portion of the packetized data stream includes the first portion of the packetized data stream representing audio data of the program (Fig.4; audio buffer memory 25; col.9, lines 4-14);

b) as discussed in claim 1 above, Suzuki fails to explicit disclose storing the second portion of the packetized data stream includes the second portion of the pascketized data stream representing audio data of the program. Official Notice is taken that it would have been obvious to modify Suzuki by adding a storage means to Suzuki in order to store the decoded audio and timing data output of the audio decoder 30.

Suzuki further discloses accessing the audio data of the first portion of the packetized data stream for audio playback (see Fig.4, audio buffer memory 25 and

audio decoder 30 and delayed coded audio data 28 which is retrieved (played back) from the audio buffer memory 25 and output to the audio decoder 30; col.9, lines 4-14)

Regarding claim 3, Suzuki discloses the method comprising wherein the multiplexed data stream is a multiplexed packetized data stream that substantially meets an MPEG2 specifications (see col.3, lines 34-42; and col.8, lines 12-13).

Regarding claim 4, Suzuki discloses the method comprising wherein the step of storing the first portion includes storing transport stream packets (see col.3, lines 34-42; and col.9, lines 20-32).

Regarding claim 5, Suzuki discloses the method comprising wherein the step of storing the first portion includes the sub steps of determining transport stream packets containing data associated with the program and storing the transport stream packets containing data associated with the program after the step of determining (see Fig.4, audio and video separator 2, and video time stamp; col.8, lines 49-67).

Regarding claim 6, Suzki disclose the method comprising wherein the step of storing the first portion includes storing packetized elementary stream (PES) packets (see col.3, lines 34-42 and col.9, lines 20-32), here examiner reads MPEG coded video signal stream and video and audio packets as PES packets.

Regarding claim 7, the claimed limitations of claim 7 are accommodated in the discussions of claims 5&6 above.

Regarding claim 8, Suzuki discloses the method wherein the step of storing the first portion of the transport stream includes the timing data including synchronization information used for playing the program back at a real time program bit-rate (see video and audio time col.12, line 42 to col.13, line 8).

Regarding claim 9, Suzuki discloses wherein incrementing the system time indicator includes incrementing the system time indicator based upon a signal generated from multiplexed packetized data stream data received after the first time (see Fig.1; selector 110, system clock reference 3 and system time counter 101; col.10, lines 33-55), here the selector 110 selects the system clock reference, and updates the system time counter 101 by the count of the system clock reference 3.

Regarding claim 10, Suzuki discloses the method of decoding the video data of the first portion to provide a decoded video stream (see Fig.4; video decoder 50; col.8, line 61 to col.9, line 3).

6. Claims 11-13,15&16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Morinaga et al (US 6,792,000).

Regarding claim 11, Suzuki fails to explicitly disclose the method wherein receiving a multiplexed packetized data stream and decoding the video data are performed by an integrated semiconductor device. Morinaga et al teach a data processing apparatus/method and a data recording medium that are capable of simultaneous recording and reproducing of a digital satellite broadcast program, wherein when the received transport stream is to be reproduced, the switch 31 selects the received transport stream from among two transports supplied thereto and supplies it to an MVLink-IC (MVLink-IC integrated circuit 16. The MVLink-IC 16 subjects the link layer processing to the output transport stream, and supplies it to PHY-IC 17. Otherwise, the MVLink-IC supplies the output transport stream to a DEMUX 18 (see Fig.1;(MV Link-IC 16 and PHY-IC 17 of Fig.1&2; col.3, lines 19-32). It would have been obvious to modify Suzuki by realizing Suzuki with an integrated semiconductor device, as taught by Morinaga, since this provides the desirable advantage of receiving and decoding packetized data stream using an integrated semiconductor device, as an alternate means of receiving and decoding packetized data stream.

Regarding claim 12, Morinaga et al further disclose the method comprising providing the decoded video stream for display at a play back rate (see col.3, lines 60-65; col.10, lines 21-26).

Regarding claim 13, Morinaga et al further disclose the method wherein the play back rate is a real time rate (see col.5, lines 58-63 and col.13 lines 6-12).

Regarding claim 15, Morinaga et al further disclose the method wherein providing the decoded video stream for display includes determining the playback rate based upon timing data received from the multiplexed packetized data stream after the first time (see col.5, lines 58-63 and col.13 lines 6-12), here the play back rate is based on the real time rate, since Morinaga is processing real time data stream.

Regarding claim 16, Morinaga et al further disclose the method wherein the timing data received from the multiplexed packetized data stream after the first time is associated with a current real time data stream (see col.5, lines 58-63 and col.13 lines 6-12), here the play back rate is based on the current real time rate, since Morinaga is processing current real time data stream.

7. Claims 14&17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Morinaga et al and further in view of Barton et al (US 6,233,389).

Regarding claim 14, Suzuki and Morinaga disclose the method wherein the providing the decoded video data for display includes determining the playback rate based upon the clock recover data of the first portion (the recorded portion) of the transport stream (see Morinaga col.12, line 56 to col.13, 11).

Suzuki and Morinaga fail to explicitly disclose the method wherein the playback rate will vary depending upon a rate at which the first portion (the recorded portion) of the transport stream data is provided to a decoder during the decoding function.

Barton et al teach time shifting of television broadcast signals, including the real time capture, storage, and display of television broadcast signals wherein a user can be watching one program while another stream is being stored (see col.4, lines 15-23, and wherein the stored program can be retrieved at a variable rate, including at a rate faster than the stored rate (see col.8, lines 19-38; col.9, lines 33-47). Playing back a stored program at a variable rate provides the desirable advantage of providing special reproduction capability to a playback system.

It would have been obvious to further modify Suzuki by realizing Suzuki with variable reproduction capability, as taught by Barton, since this provides the desirable advantage of providing special reproduction capability to a playback system.

Regarding claim 17, Barton further teaches the method wherein the playback rate is faster than a real time rate (see col.8, lines 19-38; col.9, lines 33-47.

Allowable Subject Matter

8. Claims 18-20 are allowable over the prior art of record.

9. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 18, the invention relates to time shifting of video data, including time shifting of digital video data.

The closest references Suzuki (US 6,148,135) discloses a video and audio synchronization controller for decoding coded video and audio data and for

synchronizing video data with audio data and a video decoding device in the video and audio reproducing device for preventing the video buffer memory from becoming empty (underflow) or full (overflow), and Morinaga et al (US 6,792,000) disclose a data processing apparatus/method and a data recording medium that are capable of simultaneous recording and reproducing of a digital satellite broadcast program.

However, Suzuki and Morinaga et al fail to explicitly disclose a method comprising the steps of during a third mode of operation receiving the multiplexed packetized data stream at the first demultiplexer, selecting the first program from the multiplexed packetized data stream, storing a first program portion of the first program, providing the first program portion to a second demultiplexer, selecting at the second demultiplexer a video portion of the first program portion, decoding the video portion of the first program portion for display, and storing a second program portion of the first program simultaneous to the step of decoding.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher O. Onuaku whose telephone number is (703) 308-7555. The examiner can normally be reached on M-F 8:30-6:00.

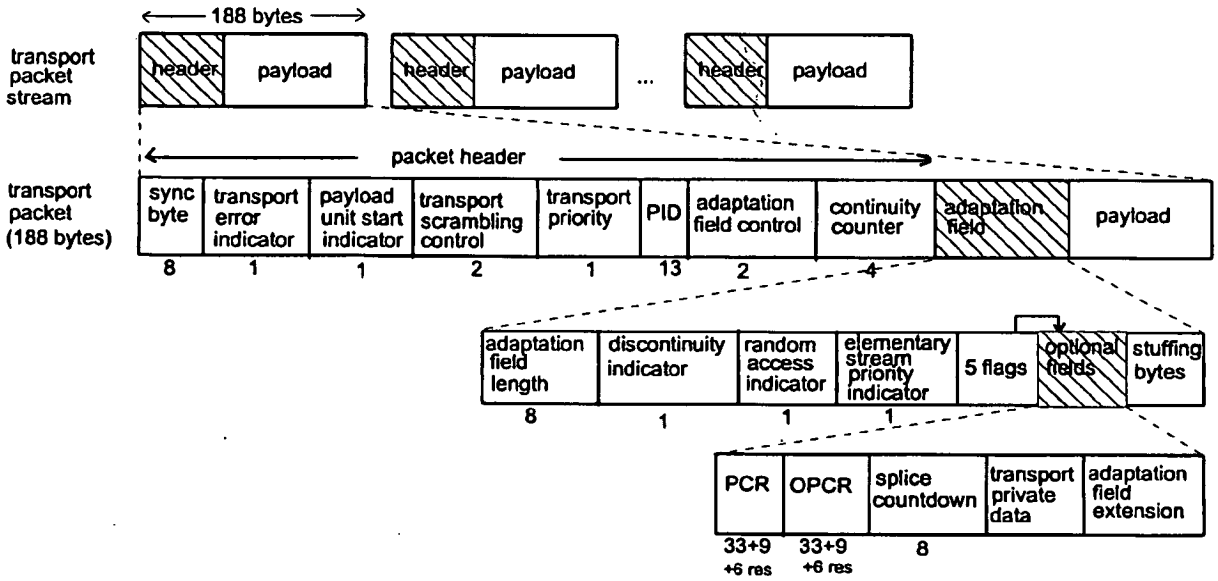
If attempts to reach the examiner by telephone are unsuccessful, the examiner's Acting supervisor, Thai Tran, can be reached on 703-305-4725. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

COO

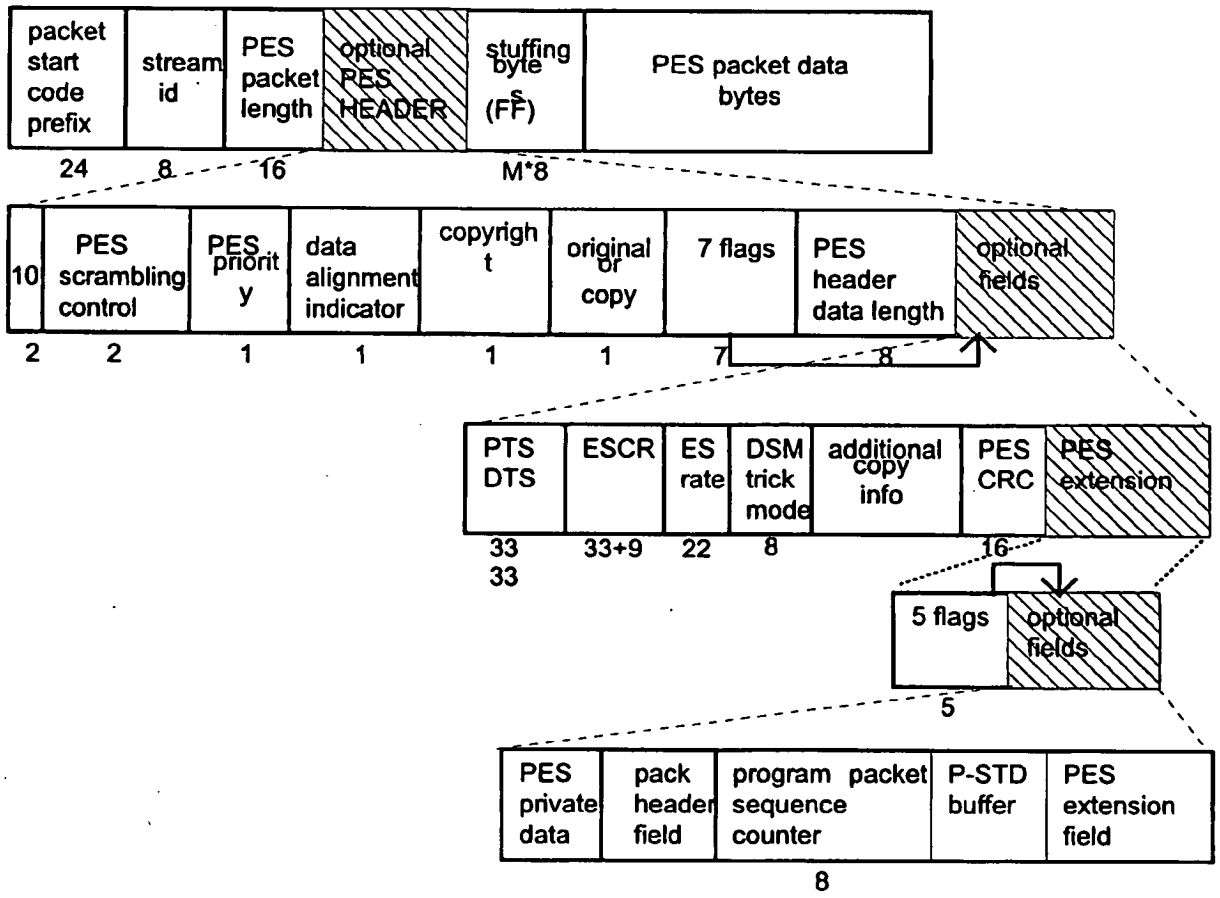
6/10/05.

James J. Groody
Supervisory Patent Examiner
Art Unit ~~262~~ 2616



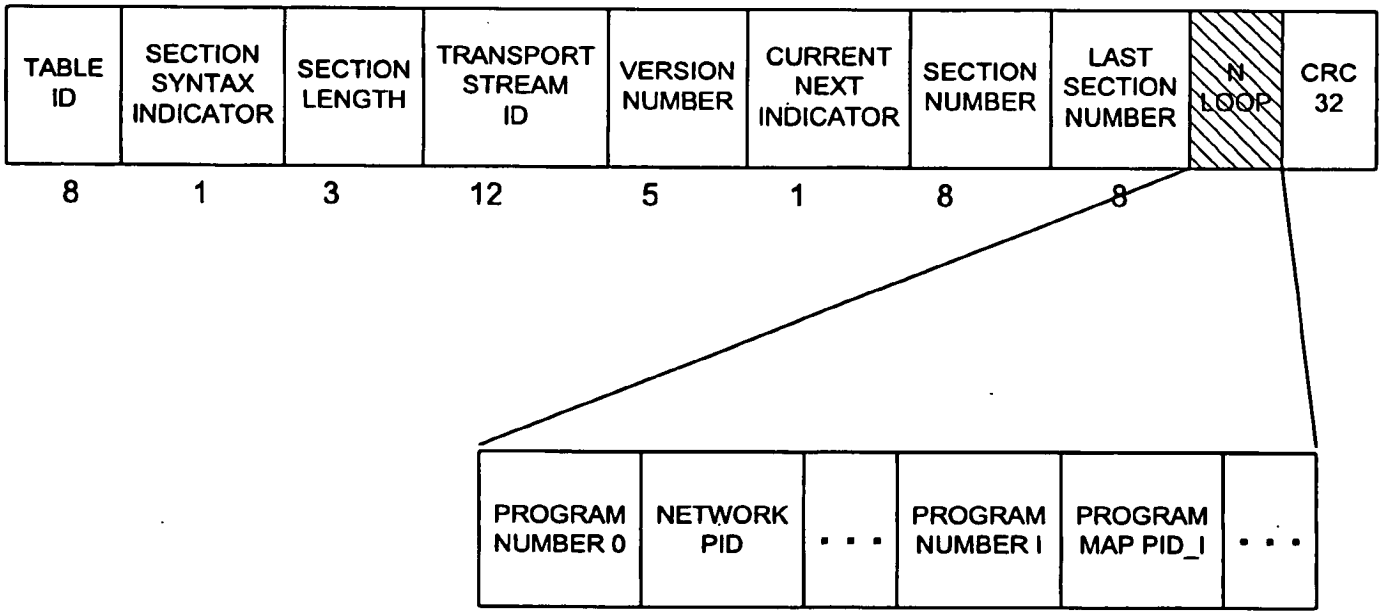
--PRIOR ART--

FIGURE 1



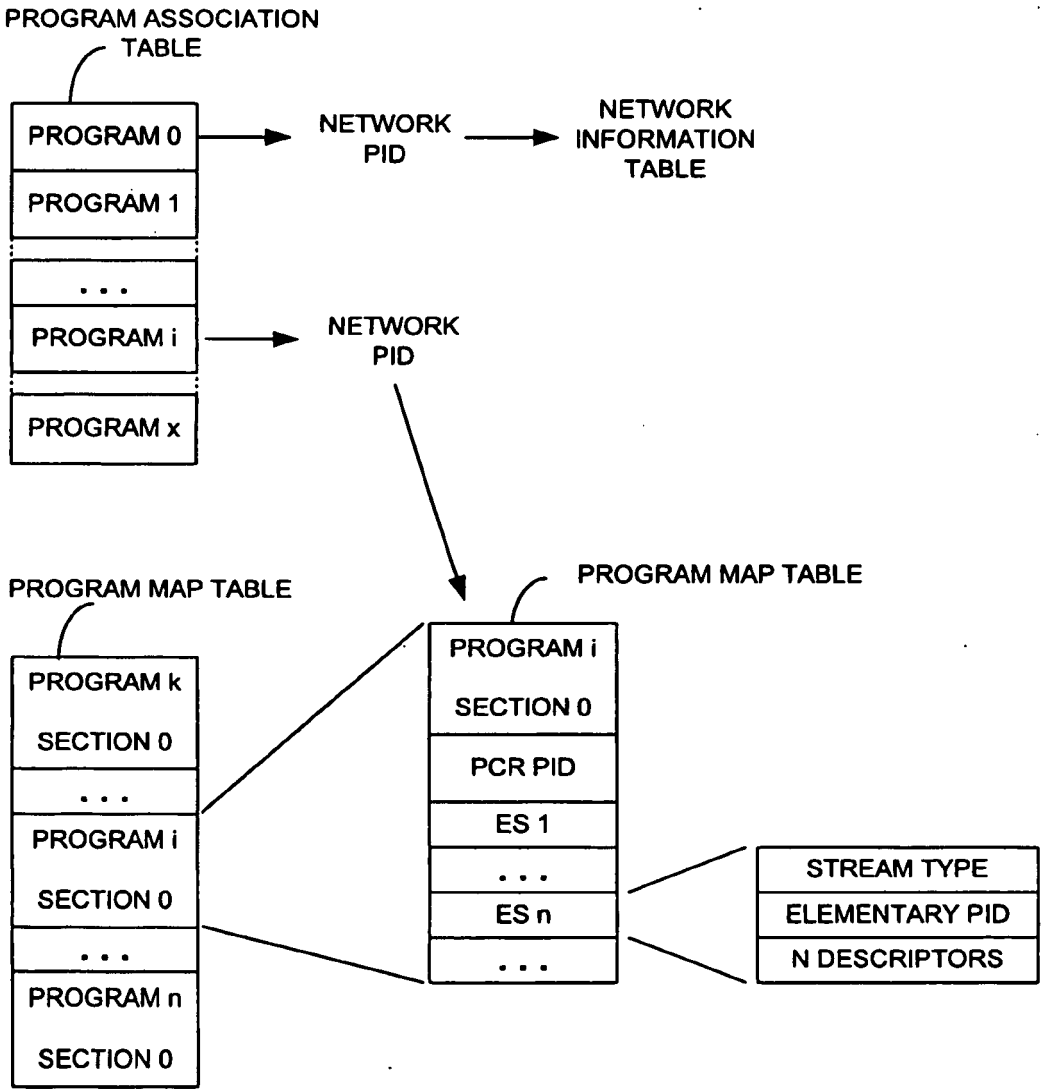
--PRIOR ART--

FIGURE 2



--PRIOR ART--

FIGURE 3



--PRIOR ART--

FIGURE 4

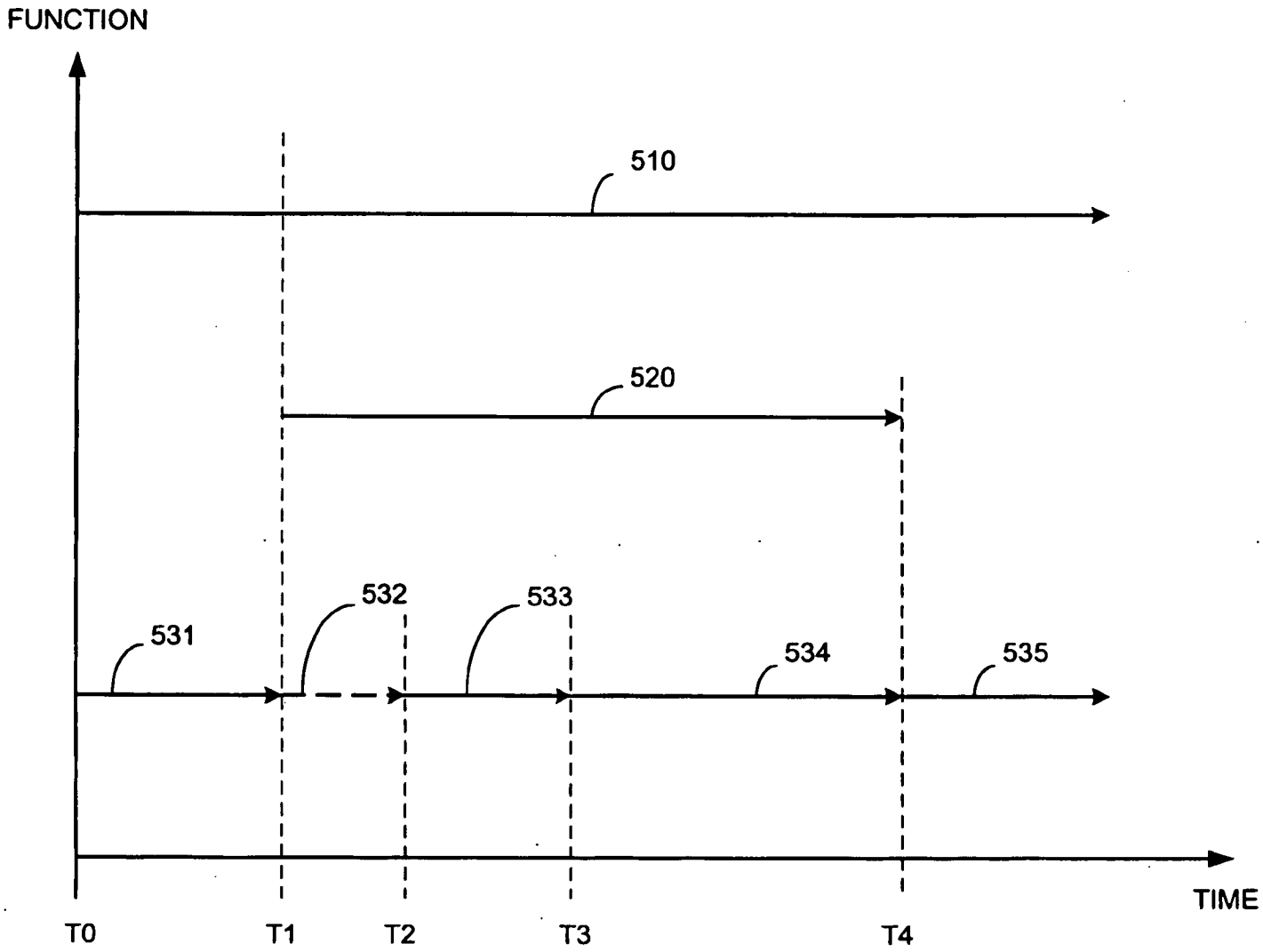


FIGURE 5

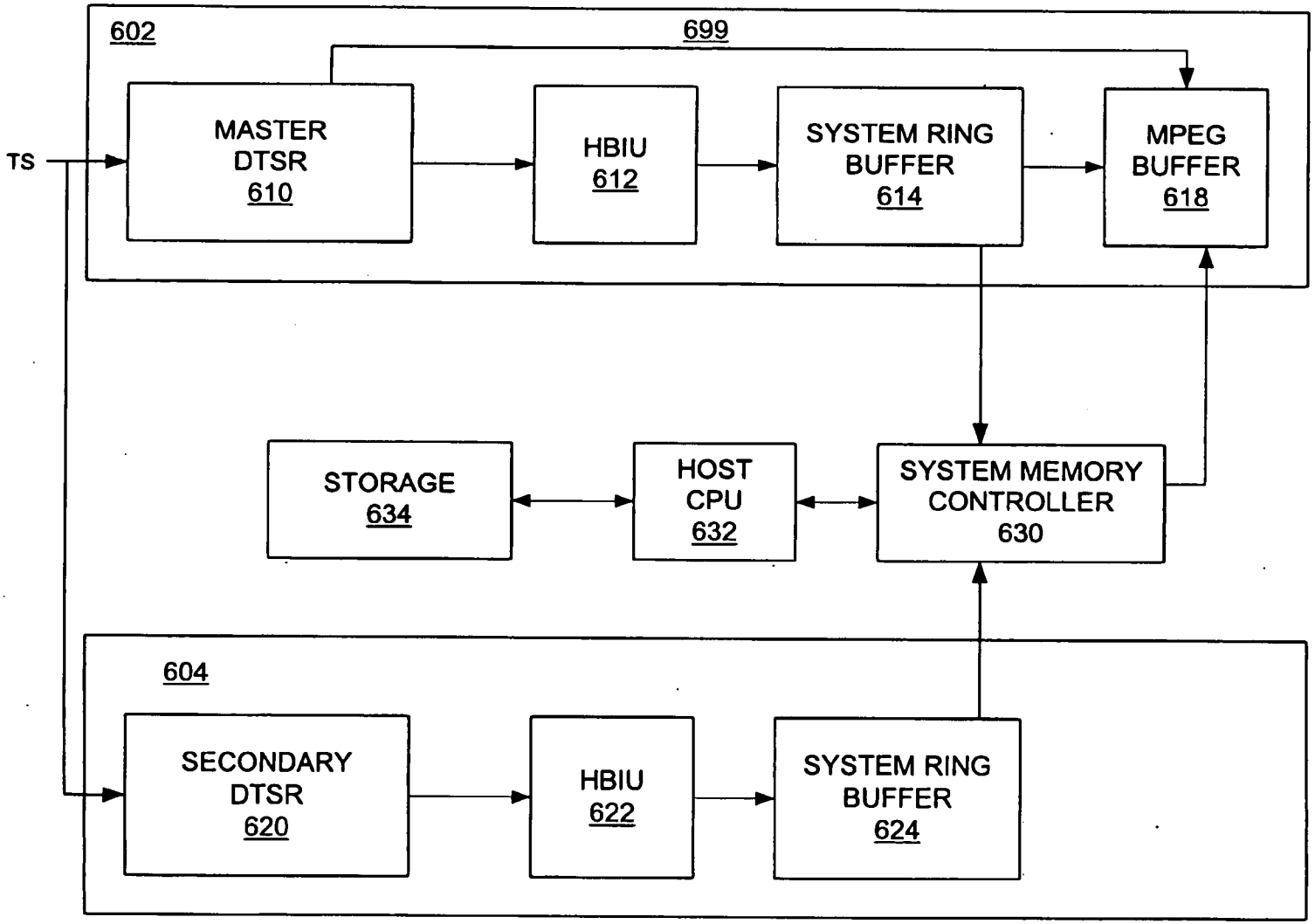


Figure 6